FORM PTO-1390 (REV 11-2000) DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NO.
851663.425USPC

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see37 CFR 1.5)
Unknown 09/830435

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/SG98/00086	**26 October 1998 (26.10.1998)**	**26 October 1998 (26.10.1998)**

TITLE OF INVENTION
MODEM ARCHITECTURE AND METHOD OF DATA TRANSFER

APPLICANT(S) FOR DO/EO/US
PAI, Pratima; DA COSTA, Godfrey; and LEONG, Foo, Yuen

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☒ A English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 – 1.825.
18. ☒ A second copy of the published international application under 35 U.S.C. 154(d)(4)
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☐ Other items of information:

U.S. APPLICATION NO (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
Unknown 09/830435	**PCT/SG98/00086**	**851663.425USPC**

21. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $860.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)..... $690.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

CALCULATIONS
PTO USE ONLY

ENTER APPROPRIATE BASIC FEE AMOUNT =				$860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$130.00	
Claims	Number Filed	Number Extra	Rate		
Total Claims	8 - 20 =	0	x $ 18.00	$.00	
Independent Claims	2 - 3 =	0	x $ 80.00	$.00	
Multiple dependent claim(s) (if applicable)			+ $270.00	$270.00	
TOTAL OF ABOVE CALCULATIONS =				$1260.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$.00	
SUBTOTAL =				$1260.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$.00	
TOTAL NATIONAL FEE =				$1260.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$.00	
TOTAL FEES ENCLOSED =				**$1260.00**	
				Amount to be refunded:	
				charged	

a. ☒ A check in the amount of $1260.00 cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. in the amount of $_ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **19-1090**. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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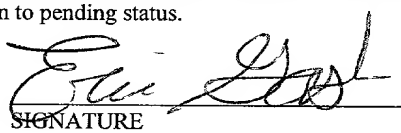


SIGNATURE

Eric J. Gash
NAME

46,274
REGISTRATION NUMBER

MODEM ARCHITECTURE AND METHOD OF DATA TRANSFER

FIELD OF THE INVENTION

The present invention relates to modem architecture and a method of data transfer for reducing on-chip Random Access Memory in a signal processor of a modem.

BACKGROUND OF THE INVENTION

Typical Modem Architectures consist of a Controller, a Datapump and hardware circuitry also called the Direct Access Arrangement (DAA), to connect to a telephone network. The Controller implements Error Control, Data Compression and digital terminal equipment (DTE) Command/Response interface.

The Datapump is arranged to perform a Datapump function which is usually specified by one of the modem standards ratified by national/international standardisation bodies, which is henceforth referred to as a Modulation function. The specific Datapump function in operation in a modem can be one of a number of Modulation functions. The Modulation functions are usually divided into phases called the Handshake phase and the Data phase. The Handshake phase pertains usually to protocol negotiation (like V.8, V.8bis), channel probing (measurement of channel characteristic), training of modem adaptive elements, and communication of modem parameters. Upon completion of the Handshake Phase, the modem enters the Data phase. These phases are usually separated by inactivity intervals.

The Datapump function (Modulation function in operation) transmits/receives data from a remote modem. The Datapump function usually requires a Digital Signal Processor (DSP) to perform the various numerical operations required for signal generation and reception. Some applications use the DSP power to accommodate the Controller function.

DSP based systems perform numerical operations on data and are optimised for such operations. A bottleneck in extracting the maximum performance is the limitation imposed by access times to memory. This is usually circumvented by providing on-chip RAM/ROM to supplement the basic DSP core. ROM based solutions preclude upgradability. Downloadable Modem architectures employ on-chip RAM for easy upgradability. This on-chip RAM is expensive compared to slower external memories like SDRAM, Flash etc.

A typical Datapump function has significant internal memory requirements. A straightforward implementation leads to an expensive single chip solution for Downloadable Modem architectures. This implies a large on-chip RAM requirement if all the program code corresponding to the Handshake and Data phase of the Modulation function were loaded in on-chip RAM.

An alternative is to provide program code for the Modulation function in external RAM, in order to free up on-chip memory and minimise costs for a single chip DSP. Figure 1 is an example of such an architecture, as used in current Modem application systems. The DSP 1 performs the Datapump function. The program code for the specific Modulation function used during a modem connection exists in external RAM 2. A slow external memory 3 stores the program code for the whole modem application. This slow external memory 3 is usually a FLASH memory, and is provided as a feature for code-version upgradability. Depending on the Modulation function used, the program code for the Datapump function is loaded into external RAM 2. The memory requirements of this Modulation function code is high because the entire code corresponding to this function is loaded. A significant problem associated with the architecture of Figure 1 is that execution of the modulation function is slowed, as compared to an on-chip DSP RAM architecture, due to the external RAM being generally slower and interfacing delays between the DSP chip and the external RAM. The present invention seeks to maximise efficiency of the DSP operation by utilizing timing constraints of operations performed by the DSP.

An example of dynamically loading or unloading tasks into instruction RAM is disclosed in EP 0 772 370. However that reference makes no mention of any timing constraints for the downloading operations performed by the DSP manager. That is likely because the downloading scheme does not require it. The ability of the DSP manager to allocate space in the data RAM in response to a request from a DSP task does not necessarily imply that inactivity timing constraints are utilized. This is because allocating space in data RAM is different from a downloading operation, it does not involve the transfer of program code from the external PC RAM to the DSP RAM.

OBJECT OF THE INVENTION

It is an object of the invention to provide an architecture and data transfer method to reduce on-chip RAM requirements in a DSP particularly, but not exclusively, in a modem whilst maintaining efficiency.

SUMMARY OF THE INVENTION

In one broad aspect of the invention, there is provided a method of data transfer for use with a signal processor of a modem, including: establishing a program code for executing a data transfer function, the function being divided into phases by inactivity intervals, and the program code including code segments associated with each phase; and downloading each code segment to a memory of the processor prior to commencement of the respective phase for execution thereof, characterised in that: each code segment is downloaded only during the associated inactivity interval.

Preferably, each successively downloaded segment overwrites a previously downloaded segment.

In another aspect, there is provided a modem architecture including: a signal processor with a first internal memory; a second memory external of the signal processor, wherein the second memory is arranged to hold a program code divided into code segments, for executing phases of a modulation function with inactivity intervals therebetween and the first memory is configured to sequentially receive the segments downloaded from the

second memory to a current segment portion of the first memory for executing same; characterised in that the modem architecture is programmed to perform the method steps, as described above.

Preferably, the signal processor is a Datapump and the first memory is provided as on-chip RAM of the Datapump.

In a more particular embodiment of the invention a Downloadable architecture is proposed which subdivides the Modulation function into phases separated by inactivity intervals. The program code segments corresponding to these phases are dynamically downloaded to on-chip RAM during the inactivity intervals without affecting the performance of the modem.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is more fully described, by way of non-limiting example only, with reference to the accompanying drawings, in which:

Figure 1 is a diagrammatic representation of a prior art Modem Datapump implementation;

Figure 2 is a diagrammatic representation of a subdivision of a Modulation Function into phases;

Figure 3 is an exemplary diagram of a single chip DSP downloadable architecture, in accordance with the invention; and

Figure 4 is a detailed diagram of the single chip DSP downloadable architecture of Figure 3.

DETAILED DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

The invention utilises a Modulation function which is subdivided into different phases as shown in Figure 2. These phases are subdivided such that there is an inactivity interval between them. Figure 2 shows the typical phases through which a Modulation function passes

through. The arrowheads 5 indicate the start of the inactivity interval. The program code for executing each phase is likewise separated into code segments (not shown), associated with each respective phase. The code segments are downloaded dynamically depending on the current phase of the Modulation function, to a DSP on-chip RAM of a Modem.

Figure 3 illustrates the proposed single chip DSP Downloadable Modem architecture. It consists of a DSP with on-chip program RAM 6. The different program segments which are to be downloaded into the on-chip RAM are stored in the slow external second memory 7.

Figure 4 presents a detailed view of the proposed Downloadable Modem architecture. A Bootloader 13 which is resident in on-chip ROM, on start-up or reset, loads an Event Arbiter Segment, Down Loader Segment, and Common Modules Segment from slow external memory 14 into the on-chip RAM 12. The initialisations of the modem system are performed by code executing from the Common Modules Segment 10. The Event Arbiter 8 monitors the current phase of the modem connection and on successful completion of the phase, requests the Down Loader 9 to download the program code segment for the next phase from slow external memory 14 into the Current Phase Segment portion 11. The Current Phase Segment code for the next phase is downloaded into on-chip DSP RAM and executed. The sequence of events that occur is further detailed using an example of a modem connection, as follows.

On start-up the Boot-loader 13, loads the modules common to all phases into the Common Modules 10. The initialisation for the modem is then performed. Depending upon the modulation function selected, Phase 1 of that modulation function is downloaded from slow external memory 14. After successful completion of Phase 1, the Event Arbiter 8 requests the Down Loader 9 to download Phase 2 from external memory into 14 the Current Phase Segment portion 11. The copied code corresponding to Phase 2 of the Datapump function overlays the existing code corresponding to Phase 1 of the Datapump function. The download operation takes place during the inactivity interval which exists between the termination of Phase 1 and the commencement of Phase 2. Phase 2 is then executed. After successful

completion of Phase 2 the Event Arbiter 8 requests the Down Loader 9 to download Phase 3 from slow external memory 14 into the Current Phase segment 11. The Current Phase Segment 11 thus has Phase 2 replaced by Phase 3. The download operation takes place during the inactivity interval which exists between the termination of Phase 2 and the commencement of Phase 3. The program for Phase 3 is then executed. This methodology is followed for the subsequent Phases of the Datapump function.

The total on-chip RAM 12 requirements includes that which is required by the Event Arbiter 8, Down Loader 9, Common Modules 10 and the Current Phase Segment 11. The memory requirements for the Current Phase Segment portion 11 is the maximum of the memory requirements of the individual phases. Thus subdivision of the Modulation Function into phases and overlaying of the code corresponding to the different Phases leads to a substantial reduction in on-chip RAM requirements in single chip DSP downloadable modem architectures.

This procedure easily incorporates inclusion of other applications by modifying the Event Arbiter 8. The new application can be loaded into the Current Phase Segment 11 when necessary. Hence a provision for integration of multiple applications which can be non-concurrently executed by the DSP is provided by this scheme. This ease in integration increases the DSP on-chip RAM requirements marginally by following the code overlay procedure for these multiple applications.

The mandatory requirement for this code overlay procedure which leads to a substantial decrease in DSP on-chip memory is the existence of inactivity intervals. Also the time required for the largest program code download should be within the duration of the inactivity intervals. Hence appropriate external slow memories which meet the latency requirements should be selected. This is exemplified by the equations given below.

The memory size of the Current Phase Segment 10 S_{max} is given by

$S_{max} = \max (S_i)$

where,

S_i is the size of the i^{th} Phase in words

The following inequality should be satisfied;

$(T_{Acc\_int} + T_{Acc\_ext} + T_{Inst\_exec}) * S_i + T_{Margin} \leq T_i$

where,

T_{Acc_ext} is the slow external memory access time

T_{Acc_int} is the on-chip RAM access time

T_{Inst_exec} is the DSP instructions execution overhead for each word transfer

T_{Margin} is the overhead for executing the Down Loader

T_i is the inactivity interval for the i^{th} Phase

This invention outlines a downloadable implementation for modem architectures which are amenable for implementation of these download procedures. Hence it is possible to achieve significant reduction in the DSP on-chip memory requirements.

The present invention provides a significant reduction in cost for single chip DSP solutions for downloadable modem applications. It outlines the procedures for downloadable implementation of the low cost single chip DSP solutions for modem applications. It also provides easy downloadability for other applications which can be executed by the DSP non-concurrently.

The above modem architecture and method has been described by way of non-limiting example only and many modifications and variations may be made thereto without departing from the spirit and scope of the invention.

THE CLAIMS:

1. A method of data transfer for use with a signal processor of a modem, including: establishing a program code for executing a data transfer function, the function being divided into phases by inactivity intervals, and the program code including code segments associated with each phase; and downloading each code segment to a memory of the processor prior to commencement of the respective phase for execution thereof, characterised in that: each code segment is downloaded only during the associated inactivity interval.

2. A method as claimed in claim 1, wherein each successively downloaded segment overwrites a previously downloaded segment.

3. A method as claimed in claim 1 or 2, wherein the data transfer function is a modem modulation function.

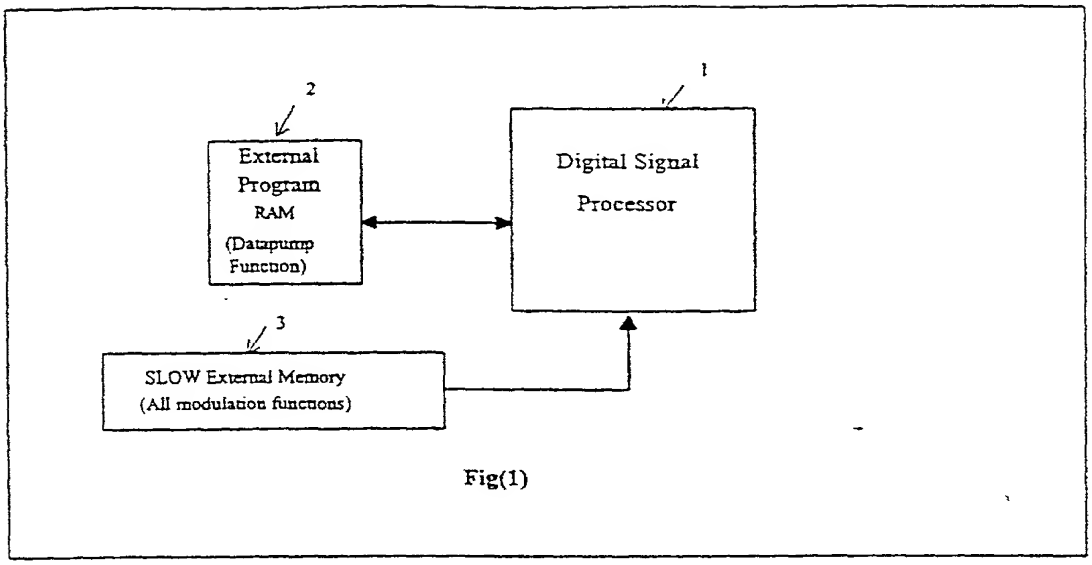
4. A method as claimed in any one of claims 1 to 3, wherein the program code is held in a second memory, external of the signal processor.

5. A method as claimed in any one of claims 1 to 4, wherein the signal processor is in the form of a Datapump.

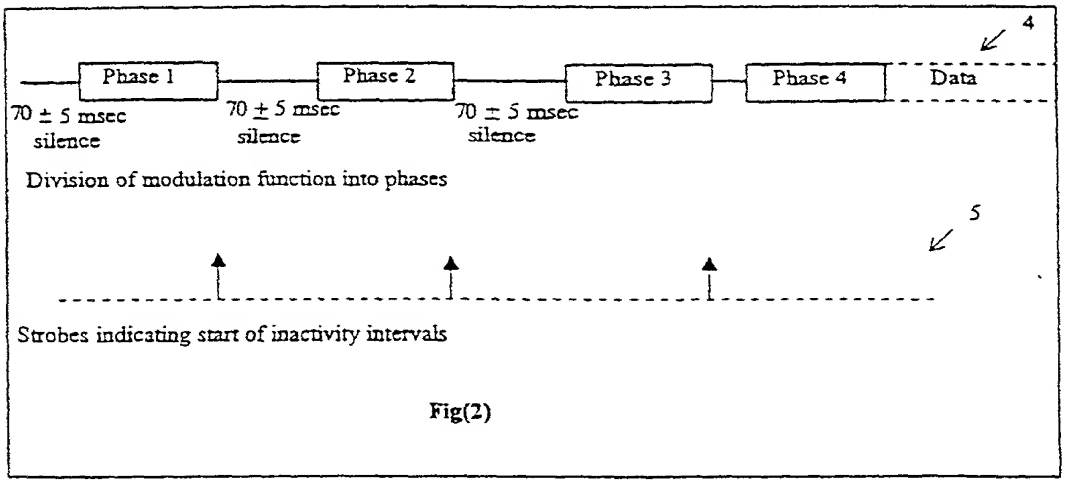
6. A modem architecture including: a signal processor with a first internal memory; a second memory external of the signal processor, wherein the second memory is arranged to hold a program code divided into code segments, for executing phases of a modulation function with inactivity intervals therebetween and the first memory is configured to sequentially receive the segments downloaded from the second memory to a current segment portion of the first memory for executing same;

characterised in that the modem architecture is programmed to perform the method steps of any one of claims 1 to 5.

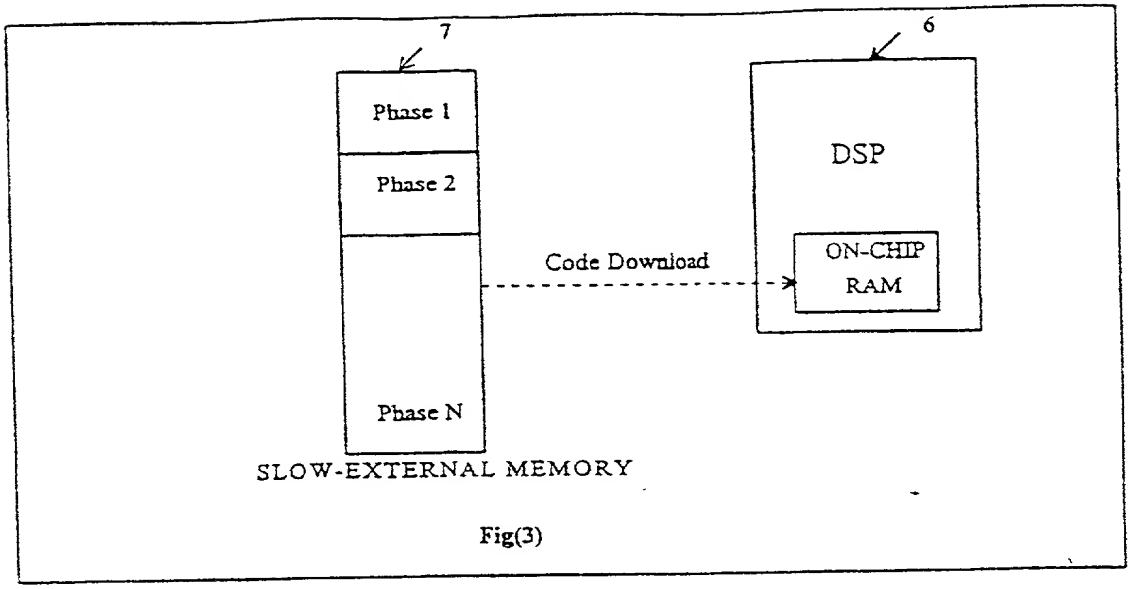
7. A modem architecture as claimed in claim 6, wherein the signal processor is a Datapump and the first memory is provided as on-chip RAM of the Datapump.


2
1
External
Program
RAM
(Datapump
Function)
Digital Signal
Processor
3
SLOW External Memory
(All modulation functions)

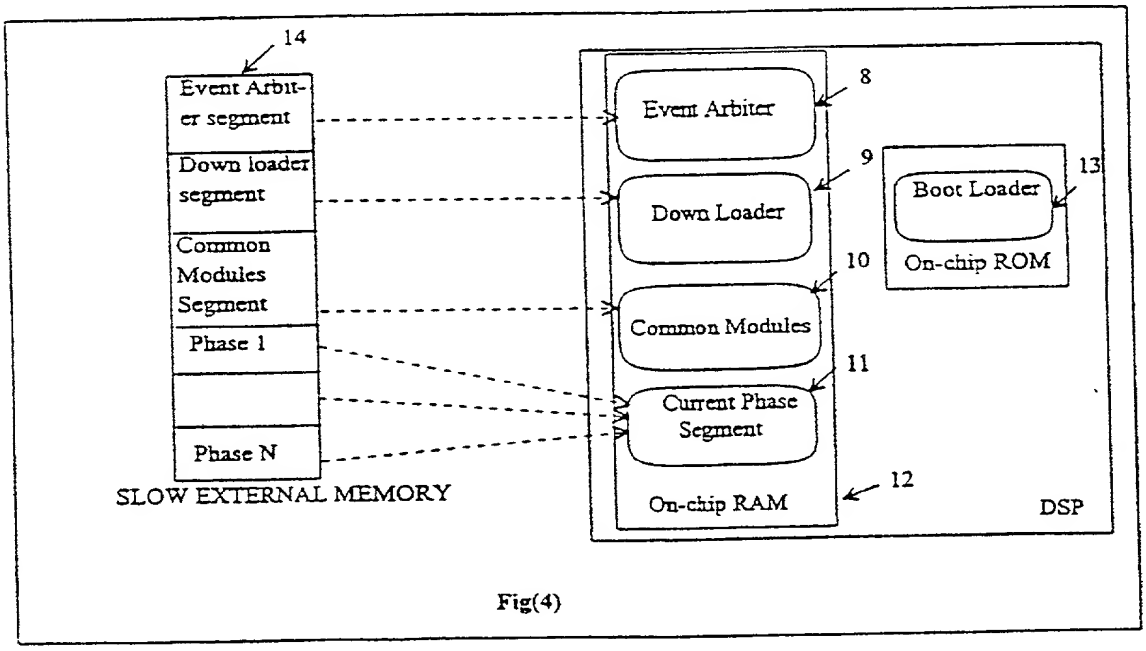
Fig(1)


4
Phase 1
Phase 2
Phase 3
Phase 4
Data
70 ± 5 msec
silence
70 ± 5 msec
silence
70 ± 5 msec
silence
Division of modulation function into phases
5
Strobes indicating start of inactivity intervals

Fig(2)


7
Phase 1
Phase 2
Phase N
SLOW-EXTERNAL MEMORY
Code Download
6
DSP
ON-CHIP RAM

Fig(3)


14
Event Arbit-er segment
Down loader segment
Common Modules Segment
Phase 1
Phase N
SLOW EXTERNAL MEMORY
Event Arbiter
8
Down Loader
9
Common Modules
10
Current Phase Segment
11
On-chip RAM
12
Boot Loader
13
On-chip ROM
DSP

Fig(4)

DECLARATION AND POWER OF ATTORNEY

As the below-named inventors, we declare that:

Our residences, post office addresses, and citizenships are as stated below under our names.

We believe we are the original, first, and joint inventors of the invention entitled "MODEM ARCHITECTURE AND METHOD OF DATA TRANSFER," which is described and claimed in the specification and claims of International Patent Application No. PCT/SG98/000086, which was filed on 26 October 1998 and for which a patent is sought.

We have reviewed and understand the contents of the foregoing specification, including the claims, as amended by any amendment specifically referred to herein (if any).

We acknowledge our duty to disclose information of which we are aware which is material to the patentability and examination of this application in accordance with 37 C.F.R. § 1.56(a).

We hereby claim foreign priority benefits under 35 U.S.C. § 119 of the foreign patent application listed below:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:			
COUNTRY	APPLICATION NUMBER	DATE OF FILING	PRIORITY CLAIMED UNDER 35 USC 119
PCT	PCT/SG98/00086	26 October 1998	Yes

We hereby appoint DAVID V. CARLSON, Registration No. 31,153; MICHAEL J. DONOHUE, Reg. No. 35,859; ROBERT IANNUCCI, Reg. No. 33,514; E. RUSSELL TARLETON, Reg. No. 31,800; ERIC J. GASH, Reg. No. 46,274; KEVIN S. COSTANZA, Registration No. 37,801; SUSAN D. BETCHER, Reg. No. 43,498; BRIAN L. JOHNSON, Registration No. 40,033; GEORGE C. RONDEAU, JR., Reg. No. 28,893; BRIAN G. BODINE, Reg. No. 40,520; CHARLES J. RUPNICK, Reg. No. 43,068; TIMOTHY L. BOLLER, Reg. No. 47,435; and FRANK ABRAMONTE, Reg. No. 38,066; comprising the firm of Seed Intellectual Property Law Group PLLC, 701 Fifth Avenue, Suite 6300, Seattle, Washington 98104-7092; and THEODORE E. GALANTHAY, Registration No. 24,122; LISA K. JORGENSON, Registration No. 34,845; ROBERT D. McCUTCHEON, Registration No. 38,717; and MARIO DONATO, Reg. No. 37,816; as our attorneys to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in

connection therewith. Please direct all telephone calls to Eric J. Gash at (206) 622-4900 and telecopies to (206) 682-6031.

We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

1-08

P Pai

Pratima Pai

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2-08

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3-CD

Foo Yuen Leong

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